Serial No. 09/611,955

IN THE CLAIMS:

Please amend claim 25 to appear as follows:

Claim 25. (Twice Amended) A semiconductor structure comprising a semiconductor substrate; recesses located in at least one major surface of said semiconductor substrate; electrical insulating layer located over said at least one major surface and in said recesses; a conductive barrier located over said insulating layer in said recesses and over said at least one major surface; a plating seed layer located over said conductive barrier within said recesses only; and a conductive metal in said recesses only.

REMARKS:

Claims 25-32 remain in the application. Applicant amended claim 25.

Applicant amended claim 25 for greater clarity, and to provide claim 25 in a better condition for possible appeal.

Applicant respectfully traverses the Examiner's rejections of the proposed Figures 1-7, and of claims 25 (as amended) -32. The application as filed fully supports the claimed invention pursuant to 35 U.S.C. 112 first and second paragraphs. Proposed Figures 1-7 merely further clarify subject matter contained in the application as filed. See, for example, page 7, line 18, among other locations, wherein the substrate is described. See, also, U.S. Patent 6,140,234 (parent ~~application, copy attached~~).